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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,486	06/28/2001	Stephen R. Mooney	884.513US1	5919

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,486	MOONEY ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *1 and 18* is/are withdrawn from consideration.

5)☒ Claim(s) *2-8 and 19-28* is/are allowed.

6)☒ Claim(s) *9-13,16 and 17* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/07/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 13 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 13 recites the limitation "the first and second current sources" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 16 recites the limitation "the first and second current sources" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 17 recites the limitation "the first and second current sources " in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 9-12 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Leung et al. (U.S. Patent No. 5,799,051).

In reference to claim 9, Leung discloses in Figure 2 a clock recovery circuit comprising: an input clock node (42) and an output clock node: a first circuit (52) to generate multiple clock phases (58) from a clock signal (RCLK) on the input clock node (42); a phase detector (128) and control circuit (120, 130, 124a, 126a) to compare a phase of a data signal and a phase of a clock signal on the output clock node (output of buffer 126a), and to create interpolator control signals (output of accumulator); and an interpolator circuit (122a) with a plurality of differential transistor pairs (320, 330 see Figure 11) operative to switch current responsive to the multiple clock phases and interpolator control signals, to drive an output clock on the output clock node.

In reference to claim 10 Leung discloses in Figure 11 wherein the interpolator circuit comprises: a first differential transistor pair (320) responsive to a first clock phase (248), and a second differential transistor pair responsive to a second clock phase (268).

In reference to claim 11, Leung discloses in Figure 11 wherein the interpolator further comprises a first current source (328) coupled to the first differential transistor pair (320); and a second current source (338) coupled to the second differential transistor pair (330).

In reference to claim 12, Leung discloses in Figure 11 wherein the first and second current sources (328, 338) are variable current sources responsive to the interpolator control signals (218, 220). The same applies to claim 17.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 9-11, 13, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Wente (U.S. Patent No. 6,438,721).

In reference to claim 9, Wente discloses in Figure 1 a clock recovery circuit comprising: an input clock node and an output clock node: a first circuit (14, 18) to generate multiple clock phases from a clock signal on the input clock node; a phase detector (12) and control circuit (20) to compare a phase of a data signal and a phase of a clock signal on the output clock node, and to create interpolator control signals (16); and an interpolator circuit (16a, 16b) with a plurality of differential transistor pairs (P1, P2 see Figure 2) operative to switch current responsive to the multiple clock phases and interpolator control signals, to drive an output clock on the output clock node.

In reference to claim 10 Wente discloses in Figure 2 wherein the interpolator circuit comprises: a first differential transistor pair (P1) responsive to a first clock phase (IN1), and a second differential transistor pair (P2) responsive to a second clock phase (IN2).

In reference to claim 11, Wente discloses in Figure 2 wherein the interpolator further comprises a first current source (T1) coupled to the first differential transistor pair (P1); and a second current source (T2) coupled to the second differential transistor pair (P2).

In reference to claim 13, Leung discloses in Figure 2 wherein the first and second current sources (T1, T2) are constant current sources responsive to the interpolator

control signals (output from 20a). The same applies to claim 16 (wherein the current sources are seen to be fixed).

Allowable Subject Matter

9. Claims 2-8 and 19-28 are allowed.

10. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: Claims 14-15 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the interpolator further includes a differential amplifier (470) coupled to the differential output nodes (410, 411) of a first *plurality of differential transistor pairs* (402, 412) and a second *plurality of differential transistor pairs* (432, 442) in combination with the rest of the limitations of the base claims and any intervening claims.

12. The following is an examiner's statement of reasons for allowance: Claims 2-8 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein each differential transistor pair (402, 412, 432, 442) is configured to receive a different phase (P0, P1, P2, P3) of a clock signal (CLOCK IN) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 19-28 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 7 wherein the integrated circuit further comprises a third differential transistor pair (706) coupled in parallel with the first differential transistor pair (702) between the

first differential output node (710, 711) and the first current source (720) in combination with the rest of the limitations of the base claims and any intervening claims. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

January 17, 2006

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800